

Serial No. 10/572,691  
Customer No. 24498  
Response dated January 06, 2012  
Reply to Office Action of November 2, 2011

PF030152

Remarks/Arguments

**Status of the Claims**

- Claims 1-11 are pending in the Application after entry of this response.
- Claims 1-11 are rejected by Examiner.
- None of Claims 1-11 has been amended by the present response.

**35 U.S.C. §103**

Claims 1 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Awamoto (US 6369514 B2) in view of Velayudhan et al. (US 6917351 B1). Applicants respectfully traverse the rejection.

As acknowledged by the Examiner, Awamoto does not teach a capacitor, a first terminal of which being coupled to the first connection line via a first switch and a second terminal of which being coupled to the second connection line (see Office Action page 5).

Velayudhan et al., has been cited to cure the deficiencies of Awamoto; however Velayudhan et al., fails to do so. Indeed, Velayudhan et al., teaches an energy recovery for a Plasma Display Panel (PDP) having a multi-phase sustain, energy being transferred between section of the PDP instead of to an external capacitor (see Abstract and Figures 6, 6A and 6B). As clearly illustrated on Figures 6, 6A and 6B, Capacitors Cp1, Cp2, Cp3 and Cp4 correspond to the capacitors forming the PDP itself and are thus included in the PDP itself, each capacitor being formed between a bulk sustain electrode X and a row scan electrode Y (see also column 6, lines 30-32 and Figure 2). As clearly stated in Velayudhan et al., at column 4, lines 48-59, the system for recapturing displacement current energy in an AC surface discharge PDP uses the PDP capacitance (Cp1 to Cp4) as a storage capacitor and external capacitors are not needed.

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In contrast to Velayudhan et al., applicants' claim 1 recites "row address means comprise separate row address means for each of the block of rows". (Emphasis added.) According to Claim 1, the "separate row address means comprising: a capacitor". (Emphasis added.) Unlike capacitors  $C_{p1}$ ,  $C_{p2}$ ,  $C_{p3}$ , and  $C_{p4}$  of Velayudhan et al., that are included in the rows of the PDP, the capacitor of Claim 1 is separate from the block of rows. It follows that the capacitor of Claim 1 cannot be properly read on any of capacitors  $C_{p1}$ ,  $C_{p2}$ ,  $C_{p3}$ , and  $C_{p4}$  of Velayudhan et al. In no way  $C_{p1}$  to  $C_{p4}$  of Velayudhan et al., correspond to the claimed capacitor (for example C1), which is external to the PDP. The capacitors  $C_{p1}$  to  $C_{p4}$  belong to the PDP 10 and not to the row scan circuitry 21, whereas the claimed capacitor (for example C1) belongs to the row address means, which is external to the PDP.

Capacitors  $C_{p1}$  to  $C_{p4}$  disclosed in Velayudhan et al., (each capacitor being formed between a bulk sustain electrode X and a row scan electrode Y) form the structure of the PDP itself, the same structure being illustrated on Figure 1 of Awamoto with row scan electrodes Y1 to Yn and sustain electrodes X1 to Xn.

Therefore, when combining the teachings of Awamoto and Velayudhan et al., a person having ordinary skill in the art would simply obtain the structure of the PDP disclosed in Awamoto.

The above mentioned topology recited with respect to the capacitor of Claim 1 provides unexpected results that are unavailable from the combination of Velayudhan et al., and Awamoto. As explained in Applicants' Specification on page 7, lines 17-20, a capacitor such as capacitor C1 that is connected between the terminals of the driver circuits guarantees in combination with the diode D1 that a correct supply voltage is maintained between the terminals of the driver circuits. Moreover, capacitor C1 provides a current path for bidirectional current coming from the panel (see for example applicants' Figures 12 and 13). Without capacitor C1, bidirectional current flowing from the panel would not be able to flow through the address means, which could generate overvoltage across the driver. Diode D1, advantageously, enables to passively regulate the voltage at the terminals of C1. It follows that Claim 1 is non-obvious in view of the combination of Velayudhan et al., and Awamoto.

Therefore, Velayudhan et al., fails to teach the separate row address means comprises a capacitor, a first terminal of which being coupled to the first connection line via a first switch and a second terminal of which being coupled to the second connection line.

It is therefore, respectfully submitted that Velayudhan et al., fails to cure the deficiencies of Awamoto and that the cited combination of Awamoto and/or Velayudhan et al., taken singly or together, fails to disclose or suggest at least "*separate row address means comprising: a capacitor, a first terminal of which being coupled to the first connection line via a first switch and a second terminal of which being coupled to the second connection line*" as claimed in pending claim 1.

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Applicant respectfully submits that pending independent claim 1 is thus not anticipated by Awamoto and/or Velayudhan et al., because not all the elements of the pending claim are found in Awamoto and/or Velayudhan et al. Also, Claims 2-11 are also not anticipated because they depend on non-anticipated independent claim 1. Applicant respectfully requests reconsideration of the 35 U.S.C. §103(a) rejection of pending Claims 1-11 based on the remarks above.

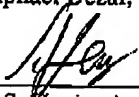
#### Conclusion

Applicant respectfully submits that the pending claims patentably define over the cited art and respectfully requests reconsideration and withdrawal of the rejections of all pending claims based on the arguments presented herein. Thus, this application stands in condition for allowance. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6812, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted.

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